An Approach to characterize the Regular Languages in TC^0 with Linear Wires

Christoph Behle, Andreas Krebs, Stephanie Reifferscheid

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Abstract

We consider the regular languages recognized by weighted threshold circuits with a linear number of wires. We present a simple proof to show that parity cannot be computed by such circuits. Our proofs are based on an explicit construction to restrict the input of the circuit such that the value computed by the circuit are constant. The result is also a corollary of [IPS93] where a different proof method based on randomized restrictions is used.

1 Introduction

Our motivation is the characterization of the regular languages in TC^0 with a linear number of wires. The study of the regular languages recognized by circuits has emerged as an important tool to understand the power of circuit classes. From this point of view the study of subclasses as TC^0 with linear wires makes sense, since it is known that each regular language can be recognized by circuits with an almost linear number of wires [CFL85, AK08]. Similar studies for the case of AC^0 and ACC^0 with a linear number of wires can be found in [KPT05].

In [IPS93] a superlinear lower bound for the number of wires needed to recognize parity with a threshold circuit of constant depth is given. The proofs of [IPS93] are based on random restriction methods.

The use of random restriction is not helpful when dealing with non commutative languages. We have developed a new method with explicit restrictions which gives us more freedom in selecting the restriction and apply it to show that parity cannot be recongized. We hope that this method can be applied to non commutative languages, e.g. the language $(e^*ae^*be^*)^*$ yielding a characterization of TC^0 with linear wires.

2 Preliminaries

Circuits. A circuit is a directed acyclic graph. We call the nodes with fan-in

zero *input nodes* and the other nodes *gates*. The edges are called wires. We say a gate g is connected to a gate g' if there is a wire from g' to g.

For a circuit with n inputs each input node is labeled with i where $1 \leq i \leq n$ Each gate is either labeled by a Boolean function $f : \{0,1\}^k \to \{0,1\}$, where k is the fan-in of the node, or by a family of Boolean functions $f = (f_i)_{i \in \mathbb{N}}$, where $f_i : \{0,1\}^i \to \{0,1\}$ is an i-ary Boolean function. A gate g consults an input i, $1 \leq i \leq n$, if there is a connection from g to an input node labeled with i.

For a circuit C_n with n inputs and an input word $w \in \{0,1\}^n$ we define the values of a gate inductively as follows: An input nodes labeled with i has the value w_i. For a gate g let $v_1, \ldots, v_k$ be the nodes connected to g. If g is labeled by a k-ary Boolean function f, the value of the gate g is $f(v_1, \ldots, v_k)$, if g is labeled by a family of Boolean functions $f = (f_i)_{i \in \mathbb{N}}$, then the value of the gate g is $f_k(v_1, \ldots, v_k)$. The value of the circuit C_n is the value of the output gate.

A word w is accepted by C_n iff the value of the output gate is 1. A language $L \subseteq \{0,1\}^*$ is recognized by a family of circuits $(C_n)_n$, where C_n has n inputs, if $C_{|w|}$ accepts w iff $w \in L$.

The depth of a circuit C_n is the length of the longest directed path in it. A family of circuits $C = (C_n)_n$ has constant depth if there is a constant d such that the depth of each circuit is bound by d. For a circuit family $C = (C_n)_n$ we define the size as follows: $size(C) : \mathbb{N} \to \mathbb{N}$ where n maps to the number of nodes of C_n.

We denote by TC^0 the class of languages recognizable by families of constant-depth polynomial size circuits consisting of unbounded weighted threshold gates. LTC^0 is the subclass of TC^0 being the class of languages recognized by linear size circuit families with linear fan-in. If we further restrict the number of wires to be linear we obtain the class WLTC^0.

A *weighted threshold gate* with k binary inputs $x_i \in \{0,1\}$ $1 \leq i \leq k$ is defined by a value $t \in \mathbb{N}$, the threshold, and k weight functions $f_i : \{0,1\} \to \mathbb{N}$. The output of the gate is 1 if $\sum_{i=1}^{k} f_i(x_i) > t$ and 0 otherwise. The usual definition of threshold gates allows as f_i only the identity function. One can also think of the weight functions to be defined on the wires instead of the gates. It should be further noted that we do not use AND, OR, or NOT gates. AND and OR gates can be simulated by using the appropriate threshold. We can avoid NOT gates by flipping the values of the appropriate weight functions of the subsequent gates.

We consider circuits over the binary alphabet $\{0,1\}$. Thus we assume to have n input gates labeled by $i \in \{1 \ldots n\}$. For an input word $w_1 \ldots w_n \in \{0,1\}^n$ the input gate i has the value w_i.

Without loss of generality we can assume that gates are either connected only to input gates or only to threshold gates, we simply add buffer gates in the other case.

Algebra. The variety **DA**, which is contained in **A**, the variety of all monoids not containing a group, and can be characterized by the condition that a monoid M is in **DA** if for all $x, y, z \in M$ $(xyz)^\omega y(xyz)^\omega = (xyz)^\omega$. The variety **DA** has been extensively studied, see for example [TT02], where also a

list of characterization for **DA** is given. In this paper we will use the following characterization of **DA**: Let $(ab)^*$ be the *bicycle language* and let B be its syntactic monoid. Then **DA** is the largest variety in **A** that does not contain B ([Alm95]).

3   Results

The main achievement of this paper is the presentation of a new proof using only simple combinatorics for the following theorem, also proved in [IPS93]. It is clear that parity can be recognized by a TC^0 circuit with a linear number of gates.

Theorem 1. *The language L_{parity} is not in $WLTC^0$.*

Since the proof of the theorem above works for any cyclic group, this has the direct consequence that:

Corollary 1. *If a regular language with neutral letter is in $WLTC^0$, then its syntactic monoid is aperiodic.*

In Theorem 14 of [KPT05] it was shown that a regular language with neutral letter is in WLC^0 iff its syntactic monoid is in **DA**. Since every AND-gate and OR-gate is can be simulated by a threshold gate the all languages with neutral letter and a syntactic monoid in **DA** are also on $WLTC^0$.

We let $L_{bicycle}$ be the language $(ab)^*$ together with a neutral letter e, i.e. $e^*(ae^*be^*)^*$.

Conjecture 1. *The language $L_{bicycle}$ is not in $WLTC^0$.*

Since any variety $\mathbf{V} \subseteq \mathbf{A}$ that does contain the bicycle is contained in **DA** ([Alm95]) the above conjecture implies the following conjecture.

Conjecture 2. *The regular languages in $WLTC^0$ are exactly those whose syntactic monoid is in **DA**.*

4   Proofs

In this section we prove that the language L_{parity} is not in $WLTC^0$. Throughout this section we will only consider regular languages L that have a neutral letter e. The following construction is similar to the first step in the proof of Theorem 2.2 in [BS95].

Lemma 1. *If a language L with neutral letter is recognized by a $WLTC^0$ circuit family of depth d then there is a family of circuits in $WLTC^0$ of depth d recognizing L, such that every input is consulted only a constant number of times.*

Proof. Assume we have at most cn wires in each circuit C_n. Fix any even n, then the set S of all inputs that are consulted more than $2c$ times has size less or equal than $n/2$, otherwise we would have more than $2c \cdot n/2 = cn$ wires.

We pick any $S' \supseteq S$ with $|S'| = n/2$. We place the neutral letter to all inputs in S', since we fix only a linear amount of inputs the number of wires is still linear. This yields a circuit in WLTC^0 with $n/2$ inputs. Hence for each n we can construct a circuit with n inputs from C_{2n} that still recognizes L, but each input is consulted at most $2c$ times. $\qquad\square$

We call a gate trivial iff its fan-in is 1. In the case that every input is consulted exactly once the gates that are connected to input gates induce a partition on the inputs. We will prove that we can construct a similar situation if we know that every input is consulted at most c times.

Lemma 2. *Let $c \in \mathbb{N}$ and let C be a circuit with n inputs and such that each input is consulted at most c times. Then there is a set S of $\lfloor n/2(c+1)\rfloor$ inputs and a set G of non-trivial gates such that every input of S that is consulted by a non-trivial gate is also consulted by exactly one gate of G.*

Proof. We prove something slightly stronger, namely that we can find a set S with the two properties:

1. Every input of S that is consulted by a non-trivial gate is also consulted by exactly one gate of G.

2. If S' is the set of all inputs consulted by gates of G, then $|S'| \leq 2|S|$.

Assume S is a set of maximal size that fulfills conditions (1) and (2) and G be the set of corresponding gates. Assume $|S| < \lfloor n/(2(c+1))\rfloor$, otherwise we are done.

We know $S \subseteq S'$ and $|S'| \leq 2|S|$, and let $\bar{S}' = \{1, \ldots, n\} \setminus S'$.

Let $p \in \bar{S}'$. If there is no non-trivial gate that consults p, we can extend S by p, a contradiction. Hence there is a non-trivial gate g that consults input p. Let $\tilde{g}$ be the inputs consulted by g.

Assume that g consults more than twice as many inputs in $\bar{S}'$ than in S, i.e. $|\bar{S}' \cap \tilde{g}| > 2|S \cap \tilde{g}|$. Then the set $T = (S \setminus \tilde{g}) \cup (\bar{S}' \cap \tilde{g})$ with the set of gates $G \cup \{g\}$ fulfills both conditions and $|T| > |S|$; a contradiction: $|T| = |S| - |S \cap \tilde{g}| + |\bar{S}' \cap \tilde{g}| \geq |S| + 1/2|\bar{S}' \cap \tilde{g}|$. Also every two gates of $G \cup \{g\}$ do not consult the same input in T, so condition 1 is fulfilled for T. In order to show condition 2, we compute $T' = S' \cup \tilde{g}$, so $|T'| = |S'| + |\bar{S}' \cap \tilde{g}| \leq 2(|S| + 1/2|\bar{S}' \cap \tilde{g}|) \leq 2|T|$.

So every gate that consults k inputs in $\bar{S}'$ also consults at least $k/2$ inputs in S, and by the previous arguments every input in $\bar{S}'$ is consulted by a such a gate. This allows to give an upper bound for the inputs in $\bar{S}'$ by the inputs in S. Since every input is consulted at most c times we get $2 \cdot (c|S|) \geq |\bar{S}'| = n - |S'| \geq n - 2|S|$. We get $|S| \geq n/(2(c+1))$, a contradiction. $\qquad\square$

If C is a LTC^0-circuit such that all gates that are connected to input gates are trivial, then there is a LTC^0-circuit of lower depth that recognizes the same

language. Note that all gates with fan-in 1 compute either the identity or the not function. If the gate computes the identity function we can simply replace it by a wire. In the other case we replace it by a wire and switch the values of the weight functions of the subsequent gate.

Lemma 3. *If g is a non-trivial threshold gate that is connected to m input gates (and no other gates), then we can fix the output of g by fixing at most $\lceil \frac{1}{2}m \rceil$ of the inputs.*

Proof. Let $f_1, \ldots, f_m \in \{0,1\} \to \mathbb{N}$ be the weight functions, and $x_1, \ldots, x_m \in \{0,1\}$ be the inputs, then the output of the majority gate depends on $\sum_i^m f_i(x_i) > t$.

First we might assume that either $f_i(0) = 0$ or $f_i(1) = 0$ for all i. Otherwise we set $k_i = \min\{f_i(0), f_i(1)\}$, $f'_i = f_i - k_i$ and $k := \sum_{i=1}^m k_i$. If we use f'_i instead of f_i and $t' = t - k$ instead of t, then the function computed by the gate does not change. Note that if $t - k < 0$ then the value of g was already independent of the input.

Now we fix the output of g by fixing at most $\lceil \frac{1}{2}m \rceil$ of the inputs: If there exists a set I of inputs $|I| = \lceil \frac{1}{2}m \rceil$ and a set of assignments for the x_i with $i \in I$, such that $\sum_{i \in I} f_i(x_i) > t$, then we fix these inputs and the output is fixed. Otherwise we have for every set J of inputs with no more than $\frac{1}{2}m$ elements that there are no $\langle x_i \rangle_{i \in J}$ such that $\sum_{i \in J} f_i(x_i) > t$. Pick any set I of inputs with $|I| = \lceil \frac{1}{2}m \rceil$ and choose for $i \in I$ the x_i such that $\sum_{i \in I} f_i(x_i) = 0$. Then there are not more than $\frac{1}{2}m$ elements left arbitrary.

Then the output of the gate depends on

$$\sum_{i=1}^m f_i(x_i) = \sum_{i \in I} f_i(x_i) + \sum_{i \notin I} f_i(x_i) = \sum_{i \notin I} f_i(x_i).$$

Since $|\{1, \ldots, m\} \setminus I| \leq \frac{1}{2}m$, the sum is less or equal to t. $\qquad\square$

In the following we use the fact that for any natural number m greater than 1, we have $\lfloor \frac{2}{3}m \rfloor \geq \lceil \frac{1}{2}m \rceil$.

Given a family of circuits that accepts the parity language, we can construct a family of circuits that accepts the complement by fixing the first input to 1. With the same construction we can get from a circuit family that accepts the complement to a circuit family that accepts the parity language. Also we do not need to fix the first input but we could fix any input to 1.

On the other hand if we fix a proper subset of all inputs in a circuit family to any input, the language accepted by the remaining inputs would be still the parity language or its complement. If we fix for each n only a linear amount of inputs the number of wires will be still linear in the number of the new inputs.

Lemma 4. *Let C be a WLTC^0 circuit with $n = (k+1) \cdot (4(c+1))^c$ inputs such that every input is consulted at most c times by non-trivial gates and C has depth d. If C recognizes $L_{parity} \cap \Sigma^n$, then there is a circuit WLTC^0 C' with k inputs of depth $d-1$, that recognizes $L_{parity} \cap \Sigma^k$.*

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Proof. We do induction on c.

Assume $c = 0$, then we can obtain a circuit of depth $d - 1$.

Assume $c \geq 1$, then we apply Lemma 2 and obtain a set S of inputs and G of gates. We fix all inputs outside of S to 0, hence we have $\lfloor n/(2(c+1)) \rfloor$ inputs left. This gives a slightly modified threshold circuit with $\lfloor n/(2(c+1)) \rfloor$ inputs. In this circuit we use Lemma 3 for each (modified) gate $g \in G$, this fixing at most half of the remaining inputs. Thus we get a (again modified) circuit with $\lfloor n/(4(c+1)) \rfloor$ inputs. This circuit recognizes either L_{parity} or its complement. But since each of these inputs was consulted by no non-trivial gate or a gate of G, which was removed, we have constructed a circuit, where each input is consulted at most $c - 1$ times by non-trivial gates. Hence by induction the result follows.

The circuits constructed either accept L_{parity} or its complement. By fixing one more input, to 0 or 1 we get a circuit that accepts L_{parity}. $\square$

Finally we can prove our upper bound.

Proof of Theorem 1. Assume by contradiction that there is a family of circuits in WLTC^0 that recognizes L_{parity}. We let d be the depth of this family and c the fan-out on the input, see Lemma 1. We assume that d is minimal. Note that $d > 1$.

By Lemma 4 we can construct for each n a circuit C'_n of depth $d - 1$ from $C_{n \cdot (6(c+2))^c + 1}$ that recognizes $L_{parity} \cap \Sigma^n$. Hence (C'_n) recognizes L_{parity}, a contradiction. $\square$

5 Discussion

We have shown via the language L_{parity} that TC^0 with linear wires is strictly contained in TC^0 with linear gates. This is an analogon to a result of Koucký et al. [KPT05] who separated AC^0 with linear wires from AC^0 with linear gates via an explicit language (and similar for ACC^0).

Methods from communication complexity were used to show that gates with small communication complexity cannot recognize languages with large communication complexity. Since threshold gates have logarithmic communication complexity this method does not work in the case of TC^0. By separating via the language L_{parity} we use an opposite approach since this language has constant communication complexity.

At the moment our approach can only be applied to commutative languages. The obstacle is Lemma 3 where inputs are fixed to letters other than the neutral letter. There is hope to extend this method by fixing more inputs and thus hopefully gaining more freedom in the choice of the letters. It is an open question whether we can use such an extension to show that the bicycle is not in TC^0 with linear wires.

Another way to prove this conjecture might be a combination of our approach and the tools of communication complexity. This could be achieved by using

Lemma 2 to limit the number of gates spanning to two different subsets of the input to a constant number.

References

[AK08]   Eric Allender and Michal Koucký. Amplifying lower bounds by means of self-reducibility. In *IEEE Conference on Computational Complexity*, pages 31–40, 2008.

[Alm95]   Jorge Almeida. *Finite Semigroups and Universal Algebra*. World Scientific, Singapore, 1995.

[BS95]   David A. Mix Barrington and Howard Straubing. Superlinear lower bounds for bounded-width branching programs. *J. Comput. Syst. Sci.*, 50(3):374–381, 1995.

[CFL85]   Ashok K. Chandra, Steven Fortune, and Richard J. Lipton. Unbounded fan-in circuits and associative functions. *J. Comput. Syst. Sci.*, 30(2):222–234, 1985.

[IPS93]   Russell Impagliazzo, Ramamohan Paturi, and Michael E. Saks. Size-depth trade-offs for threshold circuits. In *STOC*, pages 541–550, 1993.

[KPT05]   Michal Koucký, Pavel Pudlák, and Denis Thérien. Bounded-depth circuits: separating wires from gates. In *STOC*, pages 257–265, 2005.

[TT02]   Pascal Tesson and Denis Thérien. Diamonds are forever: The variety DA. In *Semigroups, Algorithms, Automata and Languages, Coimbra (Portugal) 2001*, pages 475–500. World Scientific, 2002.